SYSTEM AND METHOD FOR HIGH-LEVEL TEST PLANNING FOR LAYOUT

ABSTRACT OF THE DISCLOSURE

A process and system for placement planning for test mode circuitry of an integrated circuit design. The novel method includes the steps of partitioning a scan chain of a netlist into sets of re-orderable scan cells. The netlist is passed to layout processes and therein the scan cells of the scan chain are re-ordered based on the sets. According to one embodiment of the present invention, the scan-chain is partitioned into a number of different sets based the respective clock domains, edge sensitivity types, skew tolerance levels, surrounding cone logic, reconfigurability and simultaneous output switching requirements of the scan cells. Data representative of the resulting sets are then provided to the place-and-route processes to be used as re-ordering limitations. Particularly, the re-ordering limitations restrict the rearrangement of scan cells among different sets. The placement and routing processes, however, are not restricted from rearranging the order of scan cells within the same set. The present invention thereby allows a better designed integrated circuit to be designed and fabricated.